PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04J 3/16 — A1

(11) International Publication Number: WO 98/00941

(43) International Publication Date: 8 January 1998 (08.01.98)

(21) International Application Number: PCT/US97/11291

(22) International Filing Date: 27 June 1997 (27.06.97)

(30) Priority Data:

60/020,762	28 June 1996 (28.06.96)	US
08/767,689	17 December 1996 (17.12.96)	US

(71) Applicant: DSC TELECOM L.P. [US/US]; 1000 Coit Road, Plano, TX 75075 (US).

(72) Inventors: DESCHAINE, Stephen, A.; 3326 Bluffview Drive, Garland, TX 75043 (US). ENTEZARI, Manouchehr; 5316 Weathervane Lane, Flower Mound, TX 75028 (US). KLECKA, Rudolph, B., III; 5830 Belmont Avenue, Dallas, TX 75206 (US).

(74) Agent: FISH, Charles, S.; Baker & Botts, L.L.P., 2001 Ross Avenue, Dallas, TX 75201-2980 (US).

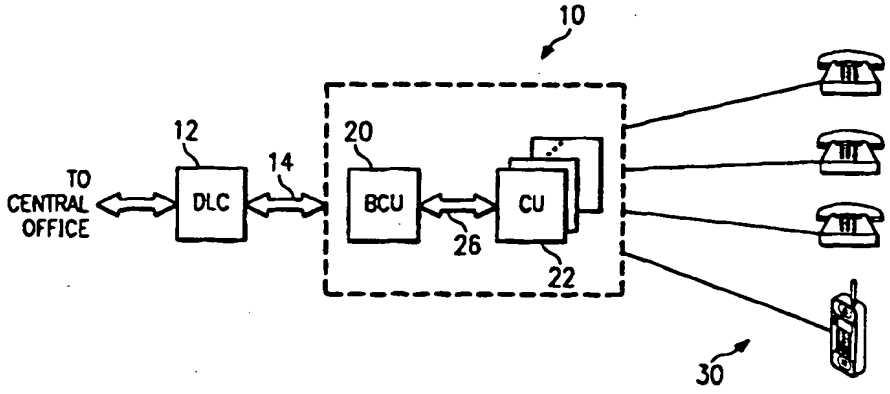
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: APPARATUS AND METHOD FOR MAPPING E1 TELECOMMUNICATIONS SIGNALS ONTO A SUBSCRIBER BUS



(57) Abstract

In a subscriber loop equipment (10) having a subscriber bus (26), there is provided an odd data stream carrying a first set of data time slots of an E1 signal and a first set of signaling and control time slots of the E1 signal, and an even data stream carrying a second set of data time slots of the E1 signal and a second set of signaling and control time slots of the E1 signal. The odd and even data streams are bit-interleaved and transported on the subscriber bus (26).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

APPARATUS AND METHOD FOR MAPPING E1 TELECOMMUNICATIONS SIGNALS ONTO A SUBSCRIBER BUS

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of telecommunications systems. More particularly, the invention is related to apparatus and method for mapping telecommunications signals onto a subscriber bus.

BACKGROUND OF THE INVENTION

In the early days of telecommunication, a copper wire medium was used to carry a single information channel. Because the greatest proportion of cost is in the materials and construction of the physical link, telephony engineers have developed ways to pack multiple channels onto a single physical link. Frequency division multiplexing (FDM) and time division multiplexing (TDM) have been devised to multiplex multiple streams of analog and pulse code modulation (PCM) digital signals, respectively, into one. For digital signals, the time division multiplexing hierarchy is DS0 through DS4, where a DS0 is a single 0.064 Mbps channel, a DS1 is 24 DS0s multiplexed together, and a DS4 is 4,032 DS0s multiplexed together.

A similar time division multiplexing scheme is used in international telephone systems based on 32-channel format, where each channel is occupied by a DS0 signal. The international digital systems, based on International Telecommunication Union CCITT's G.700 Series Recommendations, are commonly called E1 or CEPT-1. The E1

signals are based on blocks of 32 channels or time slots, of which time slot 0 and time slot 16 are typically used for control and signaling, respectively.

American telecommunications equipment manufacturers desiring to compete in the international arena must design and produce equipment that operate under the international standard. Alternatively, in order to achieve compatibility, telecommunications equipment which were originally designed and manufactured to handle signals under the American standards must be modified to accommodate international signals.

SUMMARY OF THE INVENTION

Accordingly, there is a need to provide subscriber loop equipment that are compatible with international standards, such as the transport of the E1 signal.

In one aspect of the invention, in a channel bank having a subscriber bus having a thirty-two time slot frame, there is provided an odd data stream carrying a first set of data time slots of an E1 signal and a first set of signaling and control time slots of the E1 signal, and an even data stream carrying a second set of data time slots of the E1 signal and a second set of signaling and control time slots of the E1 signal. The odd and even data streams are bit-interleaved and transported on the subscriber bus.

In another aspect of the invention, a method for mapping E1 signals onto a subscriber bus includes the steps of mapping a first set of data channels of the E1 signals onto predetermined time slots of a first data stream, and mapping a first set of signaling and control channels of the E1 signals onto other predetermined time slots of the first data stream. Further included are the steps of mapping a second set of data channels of the E1 signals onto predetermined time slots of a second data stream, and mapping a second set of signaling and control channels of

the E1 signals onto other predetermined time slots of the second data stream.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIGURE 1 is a top level block diagram of an exemplary channel bank unit constructed according to the teachings of the present invention;

FIGURE 2 is a diagram of an embodiment of a subscriber bus structure according to the teachings of the present invention;

FIGURES 3A and 3B are exemplary mapping diagrams for the subscriber bus; and

FIGURES 4A and 4B are further exemplary mapping diagrams for the subscriber bus.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment(s) of the present invention is (are) illustrated in FIGURES 1-4, like reference numerals being used to refer to like and corresponding parts of the various drawings.

Referring to FIGURE 1, a channel bank 10 constructed according to the teachings of the present invention is shown. Channel bank 10 is coupled to a digital loop carrier 12 through a data and control message link 14. Digital loop carrier 12 is in communications with equipment residing in a central office (not shown), such as a central office terminal (not shown) of the digital loop carrier and a digital cross-connect system (not shown).

Channel bank 10 is a DS0 to DS1 or DS0 to E1 multiplexing equipment primarily used for analog voice to pulse code modulation (PCM) conversion and multiplexing. Channel bank 10 includes a bank control unit (BCU) 20, which may be coupled to more than one channel unit (CU) 22 via a subscriber bus 26. Channel units 22 may operate at

DS1 and DS3 rates, as well as international rates such as E1. A plurality of subscriber equipment 30 may be coupled to each channel unit 22.

The data carried on subscriber bus 26 has the exemplary format shown in FIGURE 2. Each frame includes 32 time slots or channels, eight of which are reserved or devoted to signaling and control. In FIGURE 2, "R" denotes a reserved slot; "S1" through "S4" denote signaling time slots; "F" denotes framing; "SR" denotes systems communications service request channel; and "DL" denotes data link. In the signaling time slots of each frame, the arrows indicate the signaling time slots for the channels. The word structure for each time slot is also shown.

Subscriber bus 26 is comprised of two bit-interleaved data streams. FIGURES 3A and 3B show the data and signaling format for the ODD and EVEN data streams, which may be identical to transport two DS1 signals. Note that "sig" denotes signaling time slots. The dual DS1 or T1 mapping scheme is described in copending U.S. Patent Application titled *Apparatus and Method for Mapping Telecommunications Signals onto a Subscriber Bus*, Serial No. _____, filed on _____.

To accommodate E1 signals, two data streams are need to transport the data and signaling of one E1 signal, since it is comprised of 32 data time slots. The exemplary format for transporting the E1 signal by the ODD and EVEN data streams of a subscriber bus is shown in FIGURES 4A and 4B. Alternatively, the E1 signal may be transported on two odd data streams of two subscriber buses. It may be seen that the channels are split between the two data streams. In the embodiment shown in FIGURES 4A and 4B, 24 channels are carried on the ODD data stream, and the remaining eight channels are carried on the EVEN data stream. It may be seen that the exact mapping of the E1 channels onto the data streams may differ than shown. Further, it is contemplated that more than two data streams may be multiplexed together to form subscriber bus 26.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. In a channel bank having a subscriber bus having a thirty-two time slot frame, comprising:

an odd data stream carrying a first set of data time slots of an E1 signal and a first set of signaling and control time slots of the E1 signal;

an even data stream carrying a second set of data time slots of the E1 signal and a second set of signaling and control time slots of the E1 signal; and

the odd and even data streams being bit-interleaved and transported on the subscriber bus.

2. The channel bank, as set forth in claim 1, wherein the odd data stream comprises data time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31.

3. The channel bank, as set forth in claim 1, wherein time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31 of the odd data stream comprises data time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31, respectively.

4. The channel bank, as set forth in claim 1, wherein the even data stream comprises data time slots 0, 4, 8, 12, 16, 20, 24, and 28.

5. The channel bank, as set forth in claim 1, wherein time slots 1, 5, 9, 13, 17, 21, 25, and 29 of the even data stream comprises data time slots 0, 4, 8, 12, 16, 20, 24, and 28, respectively.

6. The channel bank, as set forth in claim 1, wherein the odd data stream comprises signaling and control time slots SRQ and DL.

7. The channel bank, as set forth in claim 1, wherein time slots 16 and 24 of the odd data stream comprises signaling and control time slots SRQ and DL, respectively.

8. The channel bank, as set forth in claim 1, wherein the odd data stream comprises signaling time slots S1-S4.

9. The channel bank, as set forth in claim 1, wherein time slots 4, 12, 20, and 28 of the odd data stream comprises signaling time slots S1-S4, respectively.

10. The channel bank, as set forth in claim 1, wherein the even data stream comprises signaling time slots S1-S4.

11. The channel bank, as set forth in claim 1, wherein time slots 4, 12, 20, and 28 of the even data stream comprises signaling time slots S1-S4, respectively.

12. A subscriber loop equipment having a bus, comprising:

an odd data stream carrying data time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31 of an E1 signal and a first set of signaling and control time slots of the E1 signal;

an even data stream carrying data time slots 0, 4, 8, 12, 16, 20, 24, and 28 of the E1 signal and a second set of signaling and control time slots of the E1 signal; and

the odd and even data streams being bit-interleaved and transported on the bus.

13. The subscriber loop equipment, as set forth in claim 12, wherein time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31 of the odd data stream comprises data time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31, respectively.

14. The subscriber loop equipment, as set forth in claim 12, wherein time slots 1, 5, 9, 13, 17, 21, 25, and 29 of the even data stream comprises data time slots 0, 4, 8, 12, 16, 20, 24, and 28, respectively.

15. The subscriber loop equipment, as set forth in claim 12, wherein the odd data stream comprises signaling and control time slots SRQ and DL.

16. The subscriber loop equipment, as set forth in claim 12, wherein time slots 16 and 24 of the odd data stream comprises signaling and control time slots SRQ and DL, respectively.

17. The subscriber loop equipment, as set forth in claim 12, wherein the odd data stream comprises signaling time slots S1-S4.

18. The subscriber loop equipment, as set forth in claim 12, wherein time slots 4, 12, 20, and 28 of the odd data stream comprises signaling time slots S1-S4, respectively.

19. The subscriber loop equipment, as set forth in claim 12, wherein the even data stream comprises signaling time slots S1-S4.

20. The subscriber loop equipment, as set forth in claim 12, wherein time slots 4, 12, 20, and 28 of the even data stream comprises signaling time slots S1-S4, respectively.

21. A method for mapping E1 signals onto a subscriber bus having thirty-two time slot frames, comprising the steps of:

mapping a first set of data channels of the E1 signals onto predetermined time slots of a first data stream;

mapping a first set of signaling and control channels of the E1 signals onto other predetermined time slots of the first data stream;

mapping a second set of data channels of the E1 signals onto predetermined time slots of a second data stream;

mapping a second set of signaling and control channels of the E1 signals onto other predetermined time slots of the second data stream; and

bit interleaving the first and second data streams.

22. The method, as set forth in claim 21, wherein the first set of E1 data channels mapping step comprises the step of mapping data channels 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31 onto the predetermined time slots of the first data stream.

23. The method, as set forth in claim 21, wherein the first set of E1 data channels mapping step comprises the step of mapping data channels 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31 onto time slots 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27, and 29-31, respectively, of the first data stream.

24. The method, as set forth in claim 21, wherein the second set of E1 data channels mapping step comprises the step of mapping data channels 0, 4, 8, 12, 16, 20, 24, and 28 onto the predetermined time slots of the even data stream.

25. The method, as set forth in claim 21, wherein the second set of E1 data channels mapping step comprises the step of mapping data channels 0, 4, 8, 12, 16, 20, 24, and 28 onto time slots 1, 5, 9, 13, 17, 21, 25, and 29, respectively, of the second data stream.

26. The method, as set forth in claim 21, wherein the first set of signaling and control channel mapping step comprises the step of mapping an SRQ and a DL signaling channels onto the other predetermined time slots of the first data stream.

27. The method, as set forth in claim 21, wherein the first set of signaling and control channel mapping step comprises the step of mapping an SRQ and a DL signaling channels onto time slots 16 and 24 of the first data stream.

28. The method, as set forth in claim 21, wherein the first set of signaling and control channel mapping step comprises the step of mapping S1-S4 signaling channels onto the other predetermined time slots of the first data stream.

29. The method, as set forth in claim 21, wherein the first set of signaling and control channel mapping step comprises the step of mapping S1-S4 signaling channels onto time slots 4, 12, 20, and 28, respectively, of the first data stream.

30. The method, as set forth in claim 21, wherein the second set of signaling and control channel mapping step comprises the step of mapping S1-S4 signaling channels onto the other predetermined time slots of the second data stream.

31. The method, as set forth in claim 21, wherein the second set of signaling and control channel mapping step comprises the step of mapping S1-S4 signaling channels onto time slots 4, 12, 20, and 28, respectively, of the second data stream.

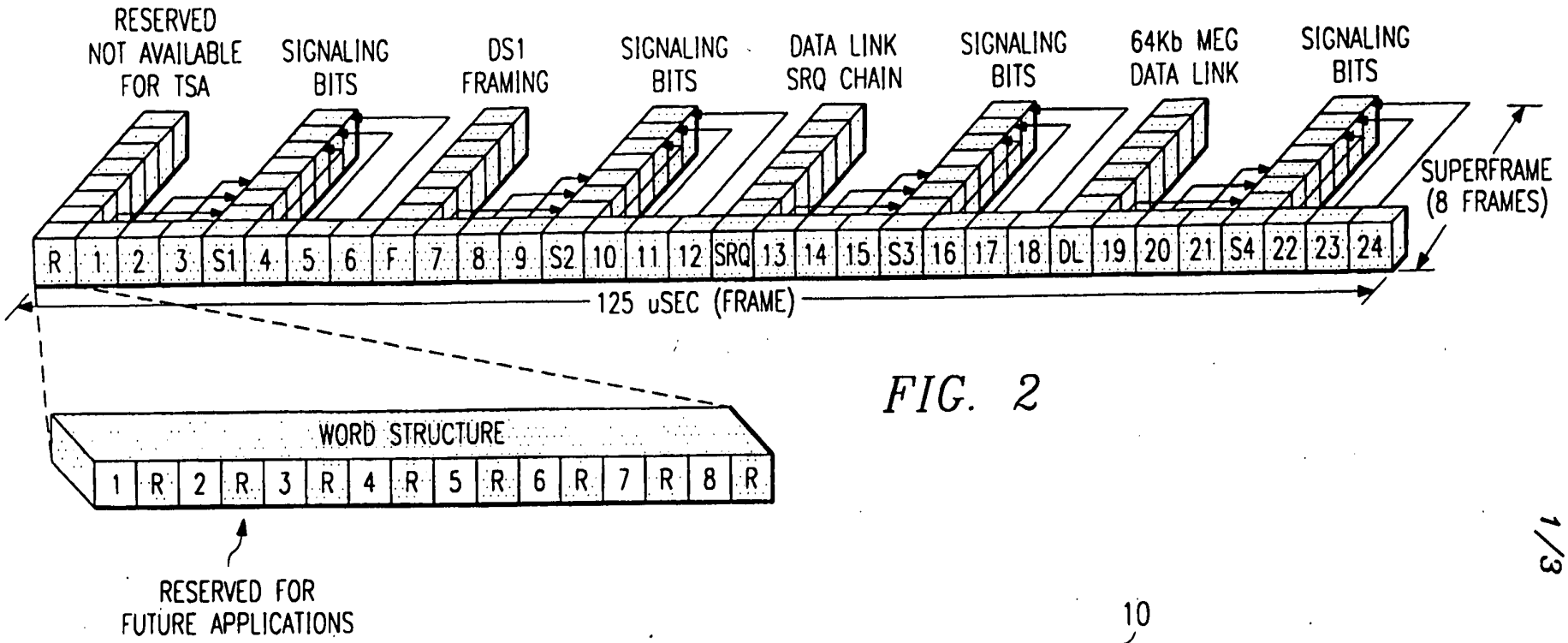

RESERVED
NOT AVAILABLE
FOR TSA
SIGNALING
BITS
DS1
FRAMING
SIGNALING
BITS
DATA LINK
SRQ CHAIN
SIGNALING
BITS
64Kb MEG
DATA LINK
SIGNALING
BITS
SUPERFRAME
(8 FRAMES)
R 1 2 3 S1 4 5 6 F 7 8 9 S2 10 11 12 SRQ 13 14 15 S3 16 17 18 DL 19 20 21 S4 22 23 24
125 uSEC (FRAME)
WORD STRUCTURE
1 R 2 R 3 R 4 R 5 R 6 R 7 R 8 R
RESERVED FOR
FUTURE APPLICATIONS

FIG. 2

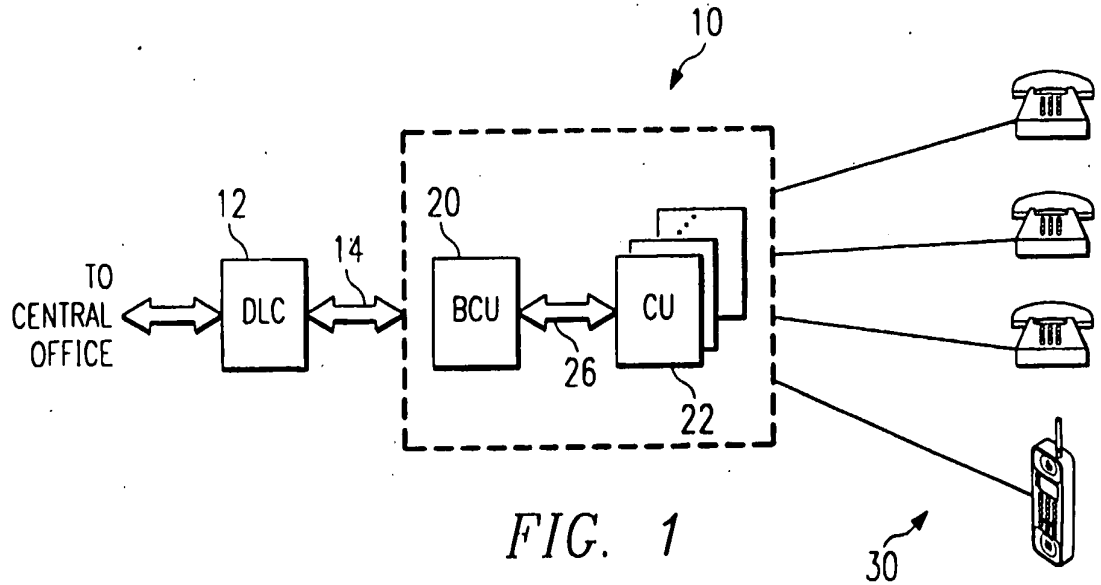

10
12
14
20
TO
CENTRAL
OFFICE
DLC
BCU
CU
26
22
30

FIG. 1

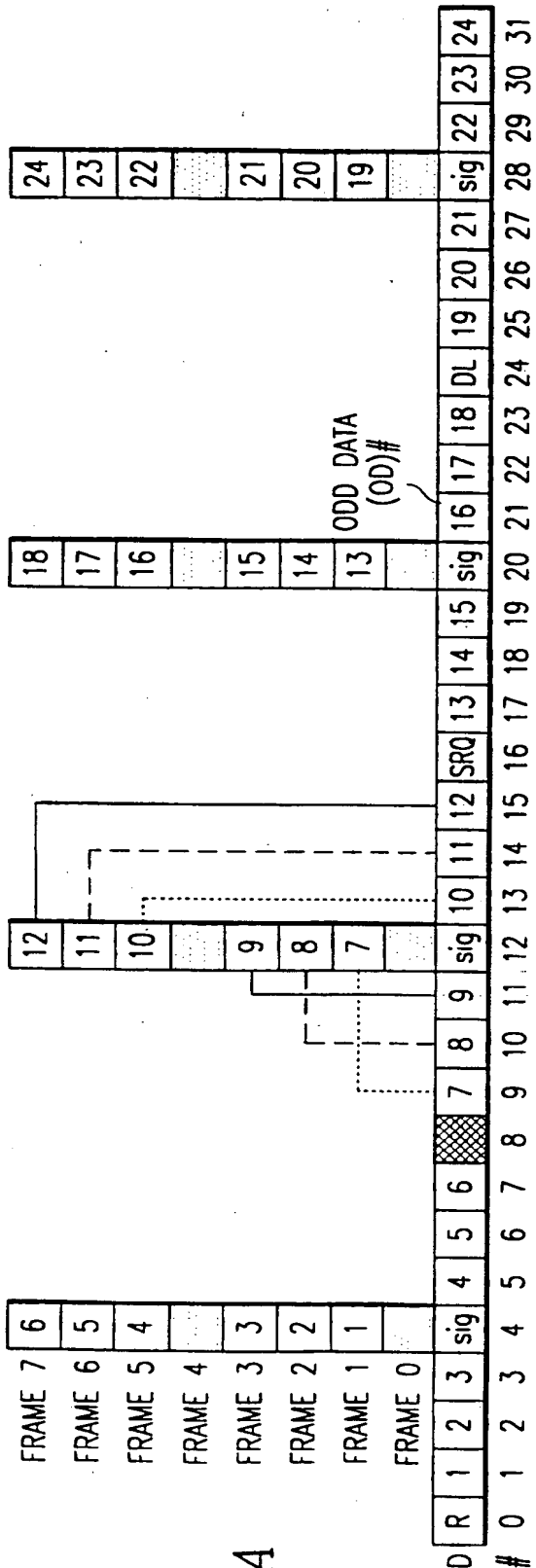

FRAME 7
FRAME 6
FRAME 5
FRAME 4
FRAME 3
FRAME 2
FRAME 1
FRAME 0
ODD
TIMESLOT #
ODD DATA (OD)#
R
sig
SRQ
DL
RESERVED
ANY DATA WITH NO SIGNALING
UNUSED

FIG. 3A

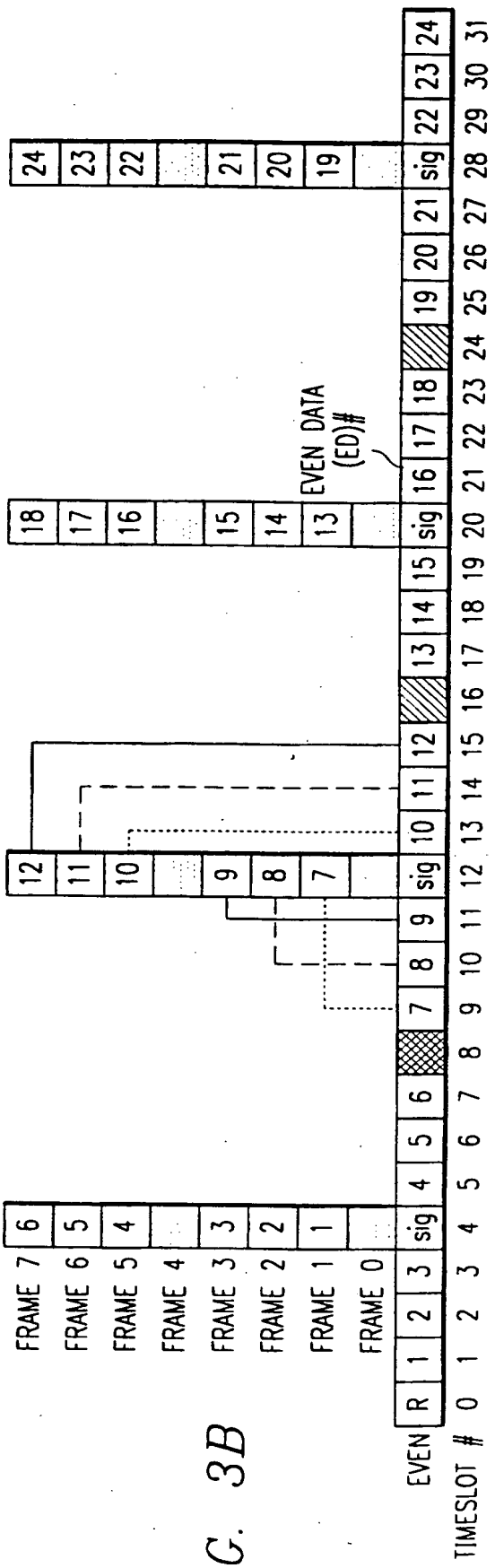
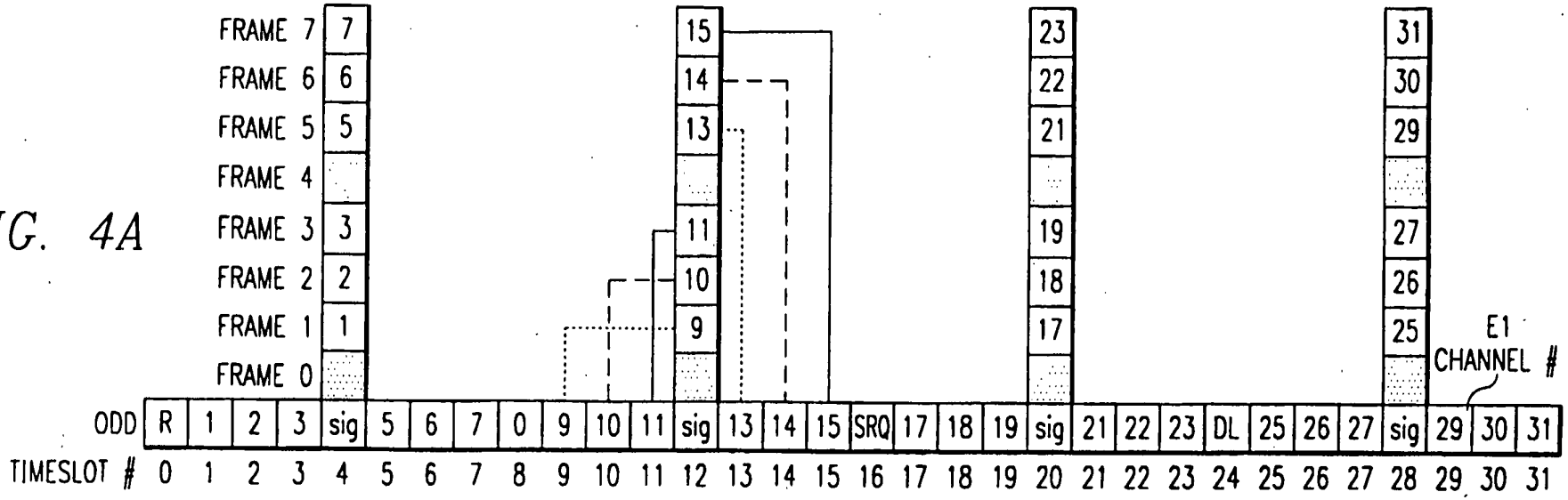

FRAME 7
FRAME 6
FRAME 5
FRAME 4
FRAME 3
FRAME 2
FRAME 1
FRAME 0
EVEN
TIMESLOT #
EVEN DATA (ED)#
R
sig

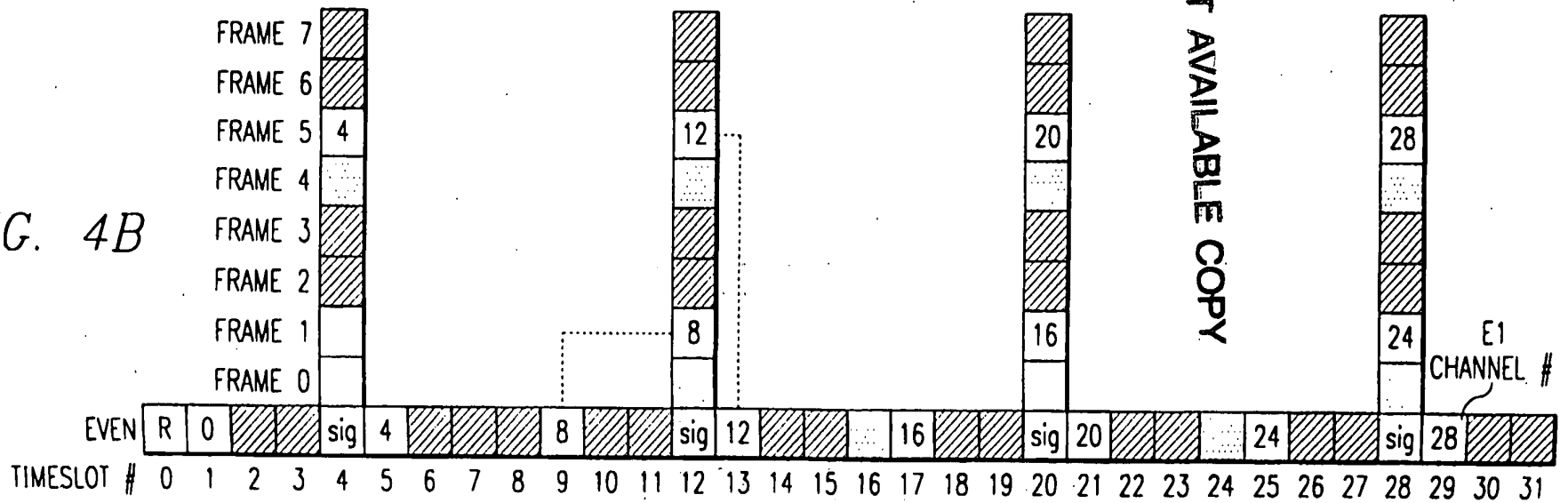
FIG. 3B

FIG. 4A



RESERVED UNUSED

FIG. 4B



INTERNATIONAL SEARCH REPORT

Internation. plication No
PCT/US 97/11291

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04J3/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2 061 673 A (INT STANDARD ELECTRIC CORP) 13 May 1981 see page 1, line 59 - page 2, line 23; figure 1 ---	1
A	GB 2 151 437 A (PLESSEY CO PLC) 17 July 1985 see page 1, line 65 - page 2, line 17 -----	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
23 October 1997	03.11.1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van den Berg, J.G.J.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internatio pplication No
PCT/US 97/11291

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2061673 A	13-05-81	BR 8006020 A	31-03-81
		US 4322844 A	30-03-82
GB 2151437 A	17-07-85	AU 573291 B	02-06-88
		AU 3648584 A	19-06-86
		FR 2556534 A	14-06-85
		US 4617659 A	14-10-86